KPR Institute of Engineering and Technology

Learn Beyond (Autonomous, NAAC "A")

Avinashi Road, Arasur, Coimbatore.

Great Place To Work. Certified MAR 2023-MAR 2024 INDIA

M.E. – VLSI Design

Curriculum and Syllabi

(Regulations – 2023)

I. Vision and Mission of the Institute

Vision

To become a premier institute of academic excellence by imparting technical, intellectual and professional skills to students for meeting the diverse needs of the industry, society, the nation and the world at large.

Mission

- Commitment to offer value-based education and enhancement of practical skills.
- Continuous assessment of teaching and learning processes through scholarly activities.
- Enriching research and innovation activities in collaboration with industry and institutes of repute.
- Ensuring the academic processes to uphold culture, ethics and social responsibilities.

II. Vision and Mission of the Department

Vision

To achieve excellence in education and research by preparing students to meet the growing needs of the society and the evolving Electronics and Communication industry.

Mission

The Mission of the Department is to

- Developing competencies in emerging technologies through skill based education collaborating with industries of repute
- Providing conducive environment for research and innovation to cater to the needs of the society.
- Instilling in students a sense of professionalism, ethical values and lifelong learning.

III. Program Educational Objectives (PEOs)

PEO1: Analyze and solve complex VLSI circuits and systems through the acquired indepth knowledge.

PEO2: Develop managerial skills and apply appropriate tools in the domains of VLSI design incorporating safety, sustainability and become a successful professional.

PEO3: Exhibit professionalism while communicating with local, national and foreign peers bound with regulations and leading life- long learning.

IV. Program Outcomes (POs)

At the end of the course, students will be able to

PO1: Apply the concepts of analog and digital circuits for IC design

PO2: Create, select and apply appropriate methods, systems and recent engineering and EDA tools including emulators for modeling and prototyping with an understanding of the tools limitations

PO3: Think laterally and originally to solve various problems in VLSI circuits and related domain after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise

PO4: Independently carry out research /investigation and development work to solve practical problems

PO5: Write and present a substantial technical report/document

PO6: Demonstrate a degree of mastery in designing, developing and testing of VLSI circuits

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V. MAPPING OF COURSE OUTCOMES WITH PROGRAM OUTCOMES

Year	SEM	Subject	PO1	PO2	PO3	PO4	PO5	PO6
I Year	SEM I	Graph Theory and Optimization Techniques	✓	✓	✓	✓	✓	✓
		Digital CMOS VLSI Design	✓	✓	✓	-	-	✓
		ASIC and FPGA Design	✓	✓	✓	-	-	✓
		Research Methodology and IPR	✓	✓	✓	-	-	✓
		Digital IC Design Laboratory	✓	✓	✓	✓	✓	✓
	SEM II	Semiconductor Device Modeling	✓	✓	✓	-	-	✓
		Analog Integrated Circuits Design	✓	✓	✓	-	-	✓
		Hardware Verification Techniques	✓	✓	✓	-	-	✓
		Analog IC Design Laboratory	✓	✓	✓	✓	✓	✓
		Technical Seminar	✓	✓	✓	✓	✓	✓
II Year	SEM III	Project Work – Phase I	✓	✓	✓	✓	✓	✓
	SEM IV	Project Work – Phase II	✓	✓	✓	✓	✓	✓
PE		CAD for VLSI Circuits	✓	✓	✓	-	-	✓
		Advanced Nano Electronic Device Fabrication	✓	✓	✓	-	-	✓
		Advanced Digital System Design	✓	✓	✓	-	-	✓
		Design of System on Chip	✓	✓	✓	-	-	✓
		Scripting Language for VLSI	✓	✓	✓	-	-	✓
		System Verilog	✓	✓	✓	-	-	✓
		Design of Semiconductor memories	✓	✓	✓	-	-	✓

		Testing of VLSI Circuits	✓	✓	✓	-	-	✓
		Interconnections and Packaging for VLSI	✓	✓	✓	-	-	✓
		VLSI Signal Processing	✓	✓	✓	-	-	✓
		Quantum Computing	✓	✓	✓	-	-	✓
		VLSI for Wireless Communication	✓	✓	✓	-	-	✓
		Advanced Embedded System	✓	✓	✓	-	-	✓
		Industrial Internet of Things	✓	✓	✓	-	-	✓
		Security solutions in VLSI	✓	✓	✓	-	-	✓
		Thermal analysis of Integrated Circuits	✓	✓	✓	-	-	✓
		Optimization Algorithm for VLSI	✓	✓	✓	-	-	✓
		MEMS and NEMS	✓	✓	✓	-	-	✓
		Mixed Signal VLSI	✓	✓	✓	-	-	✓
		Low Power VLSI Design	✓	✓	✓	-	-	✓

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M.E. VLSI DESIGN

REGULATIONS – 2023

CHOICE BASED CREDIT SYSTEM

CURRICULUM FOR I TO IV SEMESTERS

SEMESTER I

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1	P23MA103	Graph Theory and Optimization Techniques	BSC	3	0	0	3
2	P23VL101	Digital CMOS VLSI Design	PCC	3	0	0	3
3	P23VL102	ASIC and FPGA Design	FC	2	0	2	3
4	P23RMC01	Research Methodology and IPR	RMC	3	0	0	3
5		Professional Elective I	PEC	3	0	0	3
PRACTICALS							
6	P23VL103	Digital IC Design Laboratory	PCC	0	0	6	3
			TOTAL	**14**	**0**	**8**	**18**

SEMESTER II

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1	P23VL201	Semiconductor Device Modeling	PCC	3	0	0	3
2	P23VL202	Analog Integrated Circuits Design	PCC	3	1	0	4
3	P23VL203	Hardware Verification Techniques	PCC	2	0	2	3
4		Professional Elective II	PEC	3	0	0	3
5		Professional Elective III	PEC	3	0	0	3
PRACTICALS							
6	P23VL204	Analog IC Design Laboratory	PCC	0	0	6	3
7	P23VL205	Technical Seminar	EEC	0	0	4	2
			TOTAL	**14**	**1**	**12**	**21**

SEMESTER III

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1		Professional Elective IV	PEC	3	0	0	3
2		Professional Elective V	PEC	3	0	0	3
3		Professional Elective VI	PEC	3	0	0	3
PRACTICALS							
4	P23VL301	Project Work – Phase I	EEC	0	0	12	6
			TOTAL	**9**	**0**	**12**	**15**

SEMESTER IV

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
PRACTICALS							
1	P23VL401	Project Work – Phase II	EEC	0	0	24	12
			TOTAL	**0**	**0**	**24**	**12**

MANDATORY INTERNSHIP

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P23VLI01	Industrial Training / Internship	EEC	0	0	4	2

***Four weeks during any semester vacation from I to IV semester**

Total Credit: 68

LIST OF COURSES BASED ON ITS CATEGORY

FOUNDATION COURSES (FC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P23VL102	ASIC and FPGA Design	FC	2	0	2	3

BASIC SCIENCE COURSES (BSC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P23MA103	Graph Theory and Optimization Techniques	BSC	3	0	0	3

PROFESSIONAL CORE COURSES (PCC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1	P23VL101	Digital CMOS VLSI Design	PCC	3	0	0	3
2	P23VL103	Digital IC Design Laboratory	PCC	0	0	6	3
3	P23VL201	Semiconductor Device Modeling	PCC	3	0	0	3
4	P23VL202	Analog Integrated Circuits Design	PCC	3	1	0	4
5	P23VL203	Hardware Verification Techniques	PCC	2	0	2	3
6	P23VL204	Analog IC Design Laboratory	PCC	0	0	6	3

PROFESSIONAL ELECTIVES COURSES (PEC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P23VLP01	CAD for VLSI Circuits	PEC	3	0	0	3
2	P23VLP02	Advanced Nano Electronic Device Fabrication	PEC	3	0	0	3
3	P23VLP03	Advanced Digital System Design	PEC	3	0	0	3
4	P23VLP04	Design of System on Chip	PEC	3	0	0	3
5	P23VLP05	Scripting Language for VLSI	PEC	3	0	0	3
6	P23VLP06	System Verilog	PEC	3	0	0	3
7	P23VLP07	Design of Semiconductor memories	PEC	3	0	0	3
8	P23VLP08	Testing of VLSI Circuits	PEC	3	0	0	3
9	P23VLP09	Interconnections and Packaging for VLSI	PEC	3	0	0	3
10	P23VLP10	VLSI Signal Processing	PEC	3	0	0	3
11	P23VLP11	Quantum Computing	PEC	3	0	0	3
12	P23VLP12	VLSI for Wireless Communication	PEC	3	0	0	3
13	P23VLP13	Advanced Embedded System	PEC	3	0	0	3
14	P23VLP14	Industrial Internet of Things	PEC	3	0	0	3
15	P23VLP15	Security solutions in VLSI	PEC	3	0	0	3
16	P23VLP16	Thermal analysis of Integrated circuits	PEC	3	0	0	3
17	P23VLP17	Optimization Algorithm for VLSI	PEC	3	0	0	3
18	P23VLP18	MEMS and NEMS	PEC	3	0	0	3
19	P23VLP19	Mixed Signal VLSI	PEC	3	0	0	3
20	P23VLP20	Low Power VLSI Design	PEC	3	0	0	3

RESEARCH METHODOLOGY & IPR COURSES (RMC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P23RMC01	Research Methodology and IPR	RMC	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P23VL205	Technical Seminar	EEC	0	0	4	2
2	P23VL301	Project Work – Phase I	EEC	0	0	12	6
3	P23VL401	Project Work – Phase II	EEC	0	0	24	12
4	P23VLI01	Industrial Training / Internship	EEC	0	0	0	2

VIII. Scheme of Credit distribution – Summary

S. No.	Stream	Credits/Semester				Credits	Suggested by AICTE
		I	II	III	IV		
1.	Foundation Courses (FC)	3	-	-	-	3	3
2.	Basic Science Courses (BSC)	3	-	-	-	3	-
3.	Professional Core Courses (PCC)	6	13	-	-	19	20
4.	Professional Elective Courses (PEC)	3	6	9	-	18	15
5.	Research Methodology & IPR Courses (RMC)	3	-	-	-	3	3
6.	Employability Enhancement Courses (EEC)	-	2	6	12	20	28
7.	Industrial Training / Internship	-	-	-	-	2	-
Total		**18**	**21**	**15**	**12**	**68**	**69**

SEMESTER I

P23MA103	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	Category: BSC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Nil

COURSE OBJECTIVES:

- To introduce graphs as mathematical models to solve connectivity related problems
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real life situation
- To provide knowledge and training using non-linear programming under limited resources for engineering business problems

UNIT I GRAPHS 9

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths

UNIT II GRAPH ALGORITHM 9

Graph algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on graph – Theoretic algorithms – Performance of graph theoretic algorithms

UNIT III LINEAR PROGRAMMING 9

Formulation – Graphical solution – Simplex method – Big M method – Two-phase method

UNIT IV NON-LINEAR PROGRAMMING 9

Constrained problems – Equality constraints – Lagrangean method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions

UNIT V SIMULATION MODELLING 9

Monte Carlo simulation – Types of simulation – Elements of discrete event simulation – Generation of random numbers

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Douglas B. West, "Introduction to Graph theory", Pearson education, New Delhi, 2015
2. Taha, H.A., "Operations research: An Introduction", 9th edition, Pearson education, New Delhi, 2010
3. Gupta, P.K., and Hira, D.S., "Operations research", Revised edition, S. Chand and company Ltd., 2012
4. Bronson, R.,"Matrix Operation", Schaum's outline series, Tata McGraw Hill, New York, 2011

REFERENCES:

1. Sharma, J.K., "Operations research", 3rd edition, Macmillan publishers India Ltd., 2009
2. Balakrishna, R., and Ranganathan, K., "A text book of graph theory", Springer Science and Business media, New Delhi, 2012

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Apply the concepts of graph theory in solving connectivity related problems	Apply
CO2	Use the fundamental graph algorithms to solve certain optimization problems	Apply
CO3	Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems	Apply
CO4	Model various real life situations as optimization problems and effect their solution through non-linear programming	Apply
CO5	Apply simulation modelling techniques to problems drawn from industry management and other engineering fields	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	2	2	2
CO2	1	1	1	2	2	2
CO3	1	2	2	2	2	2
CO4	1	2	2	2	2	2
CO5	1	2	2	2	2	2
CO	1	1.6	1.6	2	2	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER I

P23VL101	DIGITAL CMOS VLSI DESIGN	Category: PCC			
		L	T	P	C
		3	0	0	3

PRE-REQUISITES:

- Digital logic design
- VLSI Design

COURSE OBJECTIVES:

- To learn the characteristics of MOS transistors and wire models
- To study the combinational circuit design and memory array structures
- To understand the interconnects techniques and clocking strategies.

UNIT I COMBINATIONAL CIRCUIT DESIGN 9

Pass transistor circuits – Complementary pass transistor logic – Lean integration with pass transistors – Circuit pitfalls – Silicon-on-insulator circuit design – Subthreshold circuit design

UNIT II SEQUENTIAL CIRCUIT DESIGN 9

Sequential static circuits – Klass semidynamic Flip-Flop – Differential Flip-Flops – Dual edge –Triggered Flip-Flops – Static sequencing element methodology

UNIT III CLOCKING STRATEGIES 9

Timing classification of digital systems – Synchronous interconnects – Synchronous design – Synchronous timing basics – Sources of skew and jitter – Clock-distribution techniques – Self-timed circuit design – Synchronizers and arbiters

UNIT IV DELAY MODELS 9

Timing Optimization – RC delay model – Linear delay model – Logical efforts of paths – Timing analysis delay models

UNIT V POWER STRATIGIES 9

Sources of power dissipation – Dynamic power – Activity factor, capacitance, voltage, frequency – Static power – Sources, power gating – Low power architectures

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective", 2nd edition, Prentice Hall of India, 2003
2. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". 2nd Edition, Addision Wesley,1993

REFERENCES:

1. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation", 3rd Edition, Wiley IEEE Press, 2010
2. M J Smith, "Application Specific Integrated Circuits", 1st edition, Addisson Wesley, 1997
3. John P. Uyermura, "Introduction to VLSI circuits and systems", 2nd edition, John Wiley & Sons, 2006

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain the characteristics of MOS transistors and wire models	Understand
CO2	Summarize the combinational circuits design parameters	Understand
CO3	Classify the memory and array structures	Understand
CO4	Illustrate the various interconnect techniques	Understand
CO5	Examine the timing issues in clocking strategies.	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.2	1.4	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER I

P23VL102	ASIC AND FPGA DESIGN	Category: FC			
		L	T	P	C
		2	0	2	3

PRE–REQUISITES:

- Digital Electronics

COURSE OBJECTIVES:

- To study the fundamentals of ASIC
- To understand the different FPGA architectures and interconnects
- To learn low level design languages

UNIT I BASICS OF ASIC 6

Types of ASICs – Design flow – Economics of ASICs – ASIC cell library – Combinational logic cells – Sequential logic cells – Data path cell design

UNIT II PROGRAMMABLE ASIC 6

Antifuse – Metal-metal antifuse – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX – Lattice semiconductor ECP5

UNIT III PROGRAMMABLE ASIC I/O CELLS 6

DC output –Totem pole and clamp diode – AC output-supply bounce – Transmission lines – DC input – Noise margins – Mixed voltage systems – AC Input – Metastability – Clock input – Registered inputs

UNIT IV FPGA INTERCONNECTS 6

Interconnect – Actel ACT, Xilinx LCA, Xilinx EPLD, Altera MAX 5000 and 7000, Altera MAX9000 and Altera flex

UNIT V LOW LEVEL DESIGN ENTRY 6

Schematic entry – Hierarchical design – Schematic Icons and symbols – Nets – Vectored instances and buses – Netlist screener – Low level design languages – Case studies – Implement sobel filter algorithm using HDL

LIST OF EXPERIMENTS

1. Compute the path delay of combinational logic cell by HDL synthesis
2. Design combinational logic design based on various coding styles with exhaustive test vectors
3. Analyze the latency related problems in combinational logic cell based on synthesis timing reports
4. Design Sequential logic design based on various coding styles with exhaustive test vectors
5. Compute the Interconnect delay of combinational and sequential logic cells in FPGA

Contact Periods:

Lecture: 30 Periods Tutorial: -- Periods Practical: 30 Periods Total: 60 Periods

TEXT BOOKS:

1. M.J.S.Smith, "Application Specific Integrated Circuits", 2nd edition ,Pearson Education, 2010
2. Ming-Bo Lin, "Digital System Designs and Practices using Verilog HDL and FPGAs", 7th edition, Wiley, 2012

REFERENCES:

1. Samir Palnitkar, "Verilog HDL", 2nd edition Pearson Education, 2004
2. J.Bhaskar, "A VHDL Primer", 3rd edition , Pearson- 2015
3. J.Bhaskar, "A Verilog Primer",5th edition, Prentice Hall- 2005
4. Bob Zeidman, "Designing with FPGAs and CPLDs", 4th edition, Elsevier, CMP Books, 2002
5. https://www.latticesemi.com

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Design the combinational and sequential logic cells	Apply
CO2	Illustrate the architectures of various programmable ASIC.	Understand
CO3	Infer the inputs and outputs of programming in ASIC	Understand
CO4	Compute the interconnects delay of programmable ASIC	Apply
CO5	Compare the performance of different low level design entry parameters	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.6	1.8	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER I

P23RMC01	RESEARCH METHODOLOGY AND IPR	Category: RMC			
		L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To impart knowledge in problem formulation, analysis and solutions
- To impart skills required for technical paper writing / presentation without violating professionalethics
- To familiarize knowledge on Patent drafting and filing patents

UNIT I RESEARCH PROBLEM FORMULATION 9

Meaning of research problem – Sources of research problem – Criteria characteristics of a good research problem – Errors in selecting a research problem – Scope and objectives of research problem – Approaches of investigation of solutions for research problem – Data collection – Analysis – Interpretation – Necessary instrumentations

UNIT II LITERATURE REVIEW AND DATA COLLECTION 9

Effective literature studies approaches – Analysis – Plagiarism and research ethics – Method of data collection – Types of data – Primary data – Scales of measurement – Source and collection of data observation method – Secondary data

UNIT III TECHNICAL WRITING / PRESENTATION 9

Effective technical writing – How to write report – Paper – Developing a research proposal – Format ofresearch proposal – Presentation and assessment by a review committee

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR) 9

Nature of intellectual property – Patents – Designs – Trade and copyright – Process of patenting and development – Technological research – Innovation, patenting – Development – International scenario – International co-operation on intellectual property – Procedure for grants of patents – Patenting under PCT

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR) 9

Patent rights – Scope of patent rights – Licensing and transfer of technology – Patent information and databases – Geographical indications – New developments in IPR – Administration of patent system – IPR of biological systems – Computer software etc.,

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

REFERENCES:

1. Ranjit Kumar, "Research Methodology: A Step-by-Step Guide for beginners" 2nd edition, 2014
2. Cooper, DR and Schindler, P S., "Business Research Methods", Tata McGraw Hill, 9th edition,2018
3. Robert P. Merges, Peter S, Menell, Mark A. Lemley, "Intellectual Property" in New Technological age, 2020

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Identify and formulate appropriate research problem for preferred domain	Apply
CO2	Analyze literature review and find research gaps to finalize research objectives.	Analyze
CO3	Develop the research proposal for the identified problem	Apply
CO4	Summarize the fundamentals of IPR and its process	Understand
CO5	Apply the procedures of IPR for patent publication	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	2	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	2	1	-	-	-
CO	2.8	2	1.4	-	-	2
Correlation levels:		1: Slight (Low)	2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER I

P23VL103	DIGITAL IC DESIGN LABORATORY	Category: PCC			
		L	T	P	C
		0	0	6	3

PRE–REQUISITES:

- Fundamentals of digital logic design

COURSE OBJECTIVES:

- To design and simulate various combinational circuits
- To design and implement several sequential circuits

SUGGESTED LIST OF EXPERIMENTS

I. Simulation and Implementation of combinational circuits from RTL to GDS

1. Adder and Subtractor
2. Multiplexer and Demultiplexer
3. Encoder and Decoder

II.Simulation and Implementation of sequential circuits from RTL to GDS

1. Flip Flops
2. Shift Register
3. Counters

III. Mini project

Contact Periods:

Lecture: – Periods Tutorial: – Periods Practical: 90 Periods Total: 90 Periods

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Develop HDL code for combinational circuits.	Apply
CO2	Build HDL code for sequential circuits.	Apply
CO3	Examine the backend flow of combinational circuits	Analyze
CO4	Analyze the backend flow of sequential circuits	Analyze
CO5	Utilize the different backend tools for digital circuits	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	2	3	1
CO2	3	2	3	2	3	1
CO3	3	3	3	2	3	2
CO4	3	2	3	2	3	1
CO5	3	2	3	2	3	1
CO	3	2.2	3	2	3	1.2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER II

P23VL201	SEMICONDUCTOR DEVICE MODELING	Category: PCC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Semiconductor Physics and Devices

COURSE OBJECTIVES:

- To learn device modeling and design parameters of MOSFET
- To acquaint performance parameters of semiconductor devices
- To understand the concepts of bipolar device models

UNIT I MOSFET DEVICE PHYSICS 9

Capacitances in MOS structure – Polysilicon gate work function and depletion effects – Charge in silicon dioxide – Effect of interface traps and oxide charge on device characteristics – Impact ionization and avalanche Breakdown – Band-to-band tunneling in MOSFET – Injection of hot carriersHigh-field effects in gated diode

UNIT II MOSFET MODELING 9

Long channel MOSFETs – Sub-threshold characteristics – Short channel MOSFETs – Velocity saturation and high-field transport channel length modulation – MOSFET degradation and breakdown at high fields – Device simulations in VLSI – Nodal, mesh, modified nodal and hybrid analysis equations – Solution of nonlinear networks through Newton-Raphson technique – Convergence and stability

UNIT III SCALING EFFECTS 9

MOSFET Scaling – Constant-field scaling – Generalized scaling – Non-scaling effects – Thresholdvoltage requirement – Channel profile design – Non-uniform doping – Quantum effect on thresholdvoltage

UNIT IV MOSFET KEY PARAMETERS 9

Discrete dopant effects on threshold voltage – MOSFET channel length – Extraction of effective channel length by C-V measurements – CMOS parasitic elements – Source-drain resistance, parasitic capacitances, gate resistance, interconnect R and C

UNIT V CMOS PERFORMANCE METRICS 9

Sensitivity of CMOS delay to device parameters – Delay sensitivity to channel width, length, and gate oxide thickness, supply voltage and threshold voltage – Sensitivity of delayto parasitic resistance and capacitance – Performance factors of advanced CMOS devices

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Yuan Taur, TakH Ning, "Fundamentals of Modern VLSI Devices", 2nd edition, CambridgeUniversity Press, 2013
2. B.G Streetman and S.K Banerjee, "Solid State Electronic Devices", 7th edition, Prentice Hall India,2015

REFERENCES:

1. J P Collinge, C A Collinge, "Physics of Semiconductor Devices", 2nd edition, Springer, 2006
2. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RFCMOS Circuit Design", 1st edition, John Wiley & Sons Ltd., 2003
3. S.M. Sze Kwok K. Ng, "Physics of Semiconductor Devices", 2nd edition, John Wiley & Sons, 2007
4. Arora, Narain D. "Fundamentals of Microelectronics", 2nd edition, Wiley Student Edition, 2013

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Examine the parasitic effects in MOSFET device	Analyze
CO2	Choose the suitable technique for device modeling	Apply
CO3	Explain the concepts of scaling and threshold effects in MOSFET	Understand
CO4	Understand the key parameters of MOSFET	Understand
CO5	Analyze the performance parameters of CMOS device	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	-	-	2
CO2	3	2	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	3	3	-	-	2
CO5	2	1	1	-	-	-
CO	2.6	2	1.8	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER II

P23VL202	ANALOG INTEGRATED CIRCUITS DESIGN	Category: PCC			
		L	T	P	C
		3	1	0	4

PRE–REQUISITES:

- Fundamentals of Electronic Circuits

COURSE OBJECTIVES:

- To study the basics of MOS devices and amplifiers
- To analyze the different performance parameters of operational amplifiers
- To learn the operations of bandgap references and switched capacitor circuits

UNIT I BASIC MOS DEVICE 9+3

MOSFET as a switch – Structure and symbol – MOS IV characteristics – Second order effects – MOS layout – MOS capacitance – Small signal model – Spice models – Long channel vs Short channel devices – NMOS vs PMOS – Principle of data conversion and basic circuits

UNIT II SINGLE STAGE AND DIFFERENTIAL AMPLIFIER 9+3

Common Source (CS) stage – Source Follower (SF) – Common Gate (CG) stage – Cascode Stage – Choice of device models – Single ended and differential operation – Basic differential pair – Common mode response – Differential pair with MOS load – Gilbert cell

UNIT III CURRENT MIRROR and FREQUENCY RESPONSE of AMPLIFIER 9+3

Basic current mirrors – Cascode current mirror – Active current mirrors – Biasing techniques – Miller effect – Frequency response of CS, SF and CG – Frequency response of differential amplifier – Gain bandwidth trade-offs

UNIT IV OPERATIONAL AMPLIFIER 9+3

Performance metrics – Single stage OPAMP – Double stage OPAMP – Gain boosting – Comparison – Output swing calculation – Common mode feedback – Input range limitation – Slew rate – High slew rate OPAMPs – Power supply rejection

UNIT V NANOMETER DESIGN WITH SPECIFICATIONS 9+3

Transistor design considerations – Deep submicron effects – Transconductance scaling – Nano transistor design – OPAMP design – High speed amplifiers

Contact Periods:

Lecture: 45 Periods Tutorial: 15 Periods Practical: – Periods Total: 60 Periods

TEXT BOOKS:

1. B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill Education, 2nd edition, 2016
2. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd edition, 2011

REFERENCES:

1. Paul R. Grayl, Stephen H Lewis Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, Inc., 5th edition, 2009
2. Tony Chan Carusone, David A Johns Kenneth W Martin,"Analog Integrated Design", 2nd edition John Wiley & Sons, Inc., 2012

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Summarize the characteristics and models of MOS devices	Understand
CO2	Analyze single and multistage amplifiers	Analyze
CO3	Illustrate the frequency response of different amplifiers	Understand
CO4	Examine the performance of operational amplifier	Analyze
CO5	Design amplifiers for given specification	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	2	1	1	-	-	-
CO4	3	3	3	-	-	2
CO5	3	3	3	-	-	2
CO	2.6	2.2	2.2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER II

P23VL203	HARDWARE VERIFICATION TECHNIQUES	Category: PCC			
		L	T	P	C
		2	0	2	3

PRE–REQUISITES:

- Testing of VLSI

COURSE OBJECTIVES:

- To study the concept of verification plans, tools and techniques
- To understand strategies of high level modeling and stimulus responses
- To learn the basics of architecting test benches, functional and quality verification.

UNIT I VERIFICATION TECHNIQUES AND TOOLS 6

Importance of verification – Functional verification approaches – Verification and testing comparison – Linting tools – Simulators – Waveform viewers – Issue tracking – Metrics – System Verilog

UNIT II VERIFICATION PLAN 6

Role of verification plan – Levels of verification – Strategies – Design for verification – Approaches – Universal verification and open verification methodologies

UNIT III STIMULUS AND RESPONSES 6

The parallel simulation engine – Race conditions and issues – Stimulus and outputs – Response monitor – Functional models and interfaces

UNIT IV ARCHITECTING TEST BENCHES AND SIMULATION MANAGEMENT 6

Test harness – Design configuration – Directed and random stimulus – Behavioral models – Simulation Management – Regression

UNIT V FUNCTIONAL AND QUALITY VERIFICATION 6

Need for functional verification – Methods – Random testing and co-simulation – Real world consideration – Verification plan – Applying function verification to a project

Contact Periods:
Lecture: 30 Periods Tutorial: – Periods Practical: 30 Periods Total: 60 Periods

LIST OF EXPERIMENTS

Implement a Verilog model, develop test bench and simulate the model using Cadence or model sim of the following,

1. Gate level implementation– Verify functionality, behavior and timing constraints
2. Sequential circuits– Verify functionality, behavior and timing constraints
3. Bus Functional model
4. Memory Design Verification
5. Finite state Machine
6. Coverage driven and assertion based Verification
7. Clock Domain
8. Formal Verification Error Injection and Fault Simulation

TEXT BOOKS

1. Janick Bergeron, "Writing Test benches: Functional Verification of HDL Models", 2nd edition,Springer, 2003
2. Andreas Meyer, "Principles of Functional Verification", 1st edition, Newnes, 2003

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REFERENCES

1. Samir Palnitkar, "Design Verification with E",PHI, 2003
2. Thomas Kropf, "Introduction to Formal Hardware Verification", Springer, 2010
3. Chris Spear, "System Verilog for Verification: A Guide to Learning the Testbench languageFeatures", Springer, 2008
4. Janick Bergeron, Edward Cerny, Alan Hunter and Andrew Nightingale, "Verification Methodology Manual for System Verilog", Springer, 2005

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the various techniques and tools used for verification	Understand
CO2	Summarize different verification levels and strategies	Understand
CO3	Compare the performance of simple and complex stimulus	Understand
CO4	Develop test benches using different stimuli	Apply
CO5	Examine the quality and functionality of a project in real time scenario	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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SEMESTER II

P23VL204	ANALOG IC DESIGN LABORATORY	Category: PCC			
		L	T	P	C
		0	0	6	3

PRE–REQUISITES:

- Analog electronics

COURSE OBJECTIVES:

- To simulate the analog integrated circuits using EDA tools
- To design and synthesis of CMOS circuits using EDA tools
- To design CMOS amplifier and data convertors using EDA tools

SUGGESTED LIST OF EXPERIMENTS

Simulation and Implementation from RTL to GDS using EDA tool

1. Characterization of NMOS and PMOS transistors.
2. Design of single stage Common Source (CS) and Common Drain (CD) amplifiers
3. Design of two stage op-amp based CMOS differential amplifier
4. Design CMOS current mirror circuits
5. Design of Data converters (ADC/ DAC)

Contact Periods:

Lecture: – Periods Tutorial: – Periods Practical: 90 Periods Total: 90 Periods

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Make use of cadence software for NMOS and PMOS characterization	Apply
CO2	Build various types of analog amplifiers for given specifications	Apply
CO3	Examine the performance of multi stage operational amplifiers	Analyze
CO4	Design current mirror circuits using EDA tool	Analyze
CO5	Analyze the operation of data convertor circuits	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	2	3	1
CO2	3	2	3	2	3	1
CO3	3	2	3	2	3	1
CO4	3	3	3	2	3	2
CO5	3	3	3	2	3	2
CO	3	2.4	3	2	3	1.4
Correlation levels: (High)	1: Slight (Low)		2: Moderate (Medium)		3: Substantial	

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SEMESTER III

P23VL301	PROJECT WORK – PHASE I	Category: EEC			
		L	T	P	C
		0	0	12	6

PRE–REQUISITES:

- Nil

COURSE OBJECTIVES:

- To identify the real life problems and to design solutions using the concepts of electronics and communication engineering
- To develop communication skills to work in a collaborative environment
- To demonstrate ethical and professional attributes

Contact Periods:

Lecture: – Periods Tutorial: – Periods Practical: 90 Periods Total: 90 Periods

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Formulate the specific problem statements for real life problems with the fundamental knowledge of Electronics and Communication engineering	Apply
CO2	Conduct a comprehensive literature review in the appropriate project domain	Understand
CO3	Identify the methodology and apply the suitable modern tools and techniques to get desired solution through individual and team work	Apply
CO4	Design and simulate circuits / systems / algorithms with ethical guidelines and considerations related to the project work	Analyze
CO5	Demonstrate the project through effective presentation and document the technical reports	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	1	1	-	-
CO2	-	-	1	1	2	-
CO3	2	3	2	3	-	1
CO4	2	3	3	3	-	2
CO5	-	-	-	-	3	3
CO	2.3	3	1.75	2	2.5	2
Correlation levels: (High)	1: Slight (Low)		2: Moderate (Medium)		3: Substantial	

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SEMESTER IV

P23VL401	PROJECT WORK – PHASE II	Category: EEC			
		L	T	P	C
		0	0	24	12

PRE–REQUISITES:

- Nil

COURSE OBJECTIVES:

- To identify the real life problems and to design solutions using the concepts of electronics and communication engineering
- To develop communication skills to work in a collaborative environment
- To demonstrate ethical and professional attributes

Contact Periods:

Lecture: – Periods Tutorial: – Periods Practical: 180 Periods Total: 180 Periods

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Identify, formulate and analyze the problem statements with appropriate consideration of societal needs	Apply
CO2	Design and develop solutions based on electronics and communication system using modern tools/equipment /software	Apply
CO3	Apply ethical principles and professional practices throughout the project	Apply
CO4	Analyze, synthesize the results to provide the solutions for real life problem	Evaluate
CO5	Demonstrate the working model as an individual / team and organize the results in form of technical reports	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	3	2	1	-
CO2	2	3	2	2	-	2
CO3	-	-	2	1	1	-
CO4	2	2	2	3	-	1
CO5	-	-	-	-	3	3
CO	2	2.5	2.25	2	1.6	2
Correlation levels: 1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)						

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PROFESSIONAL ELECTIVE

P23VLP01	CAD FOR VLSI CIRCUITS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design principles

COURSE OBJECTIVES:

- To understand the basic concepts of physical design and algorithms techniques
- To learn floor planning and routing
- To study simulation and high-level synthesis

UNIT I DESIGN METHODOLOGIES AND GRAPH THEORY & ALGORIHMS 9

Introduction to VLSI design flow and design methodologies – Evolution of CAD tools – Classification of CAD tools – Data structures for the representation of graph – Computational complex – Examples of graph algorithm – Depth-first search – Breadth-first search – Dijkstra's shortest-path algorithm

UNIT II PARTITIONING AND PLACEMENT 9

Layout compaction – Design rules – Problem formulation – Algorithms for constraint graph compaction – Placement and partitioning – Circuit representation – Placement algorithms – Partitioning – Group migration algorithms – Kernighan-Lin algorithm

UNIT III FLOOR PLANNING AND ROUTING 9

Floor planning concepts – Shape functions and floor plan sizing – Classification of floor planning algorithms – Constraint based floor planning – Classifications of global routing algorithms – Maze routing algorithms – Lee's algorithm.

UNIT IV SIMULATION AND LOGIC SYNTHESIS 9

Simulation – Gate level modeling and simulation – Switch-level modeling and simulation – Combinational logic synthesis – Binary Decision Diagrams (BDD)

UNIT V MODELLING AND HIGH LEVEL SYNTHESIS 9

High level synthesis – Hardware models – Internal representation – Allocation – Assignment and scheduling – Simple scheduling algorithm – Assignment problem

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Sabih H. Gerez.,"Algorithms for VLSI Design Automation" 2nd edition, John Wiley & Sons, 2006
2. Sherwani, N.A., "Algorithms for VLSI Physical Design Automation", 3rd edition Kluwer Academic Publishers, 2002

REFERENCES:

1. Charles J. alpert , Dinesh P. mehta , Sachin S. Sapatnekar "Handbook of Algorithms for Physical design Automation" CRC press,2009.
2. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", 2nd edition, World Scientific, 1999.
3. Stephen Trimberger, "Introduction to CAD for VLSI", 2nd edition, Kluwer Academic publisher, 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Illustrate various graph algorithms for optimization problems.	Understand
CO2	Choose appropriate algorithm for partitioning and placement	Apply
CO3	Identify suitable algorithms for placement and floor planning	Apply
CO4	Examine the optimized gate level representation of combinational circuits.	Analyze
CO5	Summarize hardware model for high level synthesis	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	2	1	-	-	1
CO3	3	2	1	-	-	1
CO4	3	3	3	-	-	2
CO5	2	1	1	-	-	-
CO	2.16	1.8	1.4	-	-	1.33
Correlation levels:		1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP02	ADVANCED NANO ELECTRONIC DEVICE FABRICATION	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital CMOS VLSI design

COURSE OBJECTIVES:

- To study NANO - CMOS processing technologies and sub wave length lithography process
- To understand the working of ESD models and hetrostructure for MOSFET
- To learn various simulation tools used for Hetro-FETs.

UNIT I NANO-CMOS SCALING PROBLEMS AND PROCESS TECHNOLOGY 9

Design methodology in the Nano-CMOS era – Innovations needed to continue performance scaling – Overview of sub-100-nm scaling challenges and sub wavelength optical lithography – Process control and reliability – Lithographic issues and mask data explosion – Equipment requirements for front-end processing – Front-end-device problems in CMOS scaling

UNIT II SUBWAVE LENGTH OPTICAL LITHOGRAPHY 9

Imaging theory – Challenges for the 100-nm node – Resolution enhancement techniques – Physics – Physical design style impact on RET and OPC complexity – The road ahead – Future lithographic technologies

UNIT III ELECTROSTATIC DISCHARGE PROTECTION DESIGN 9

ESD standards and models – ESD protection design – Low-C ESD protection design for high-speed I/O – ESD protection design for mixed-voltage I/O – SCR devices for ESD protection

UNIT IV STRAINED-SI HETEROSTRUCTURE MOSFETs 9

Operating principle – Uniaxial stress – Process flow – Strained-Si MOSFETs with SiC – Stressor – Biaxial strain – Process flow – Scaling of Strained-Si MOSFETs – Strained-Si MOSFETs – Reliability – Industry example – TSMC-AMD

UNIT V MODELING AND SIMULATION OF HETERO-FETS 9

Simulation of Hetero-FETs – Strained-Si material parameters for modeling – Simulation of Strained-Si n-MOSFETs – Characterization of Strained-Si Hetero-FETs – TCAD – Strain-engineered Hetero-FETs – SPICE parameter extraction

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Wong, B.P., Mittal, A., Cao Y. and Starr, G., "Nano-CMOS Circuit and Physical Design", Wiley, 2004
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., "Strained-Si and Hetrostructure Field Effect Devices", Taylor and Francis, 2007

REFERENCES:

1. Hanson, G.W., "Fundamentals of Nano electronics", Pearson Education India, 2008
2. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nan electronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press 2011
3. Lundstrom, M., "Nanoscale Transport: Device Physics, Modeling, and Simulation", Springer, 2000

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the scaling problems in CMOS process technologies	Understand
CO2	Summarize the steps involved in Lithography	Understand
CO3	Illustrate the ESD standards and models for SCR devices	Understand
CO4	Apply scaling principle for heterostructure MOSFETs	Apply
CO5	Examine the performance of simulation tools used for MOSFET modeling	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP03	ADVANCED DIGITAL SYSTEM DESIGN	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital Electronics, VLSI

COURSE OBJECTIVES:

- To design synchronous and asynchronous sequential network using different techniques
- To understand the importance of PLD and algorithms for FPGA based combinational circuits design
- To study algorithms and architectures for digital processors

UNIT I SYNCHRONOUS SEQUENTIAL NETWORKS 9

Analysis of clocked synchronous sequential networks – Modeling of clocked synchronous sequentialnetworks – State stable assignment – State table reduction – Design of clocked synchronous sequential networks – Algorithmic state machine charts

UNIT II ASYNCHRONOUS SEQUENTIAL NETWORKS 9

Analysis of Asynchronous Sequential Circuits (ASC) – Flow table reduction – Races in ASC – State assignment – Problems and the transition table – Design of ASC – Static and dynamic hazards – Essential hazards

UNIT III PLD AND ARCHITECTURES OF DIGITAL PROCESSORS 9

Introduction to PLD – Types of PLD – ROM – Organization and combinational logic design using ROM – PLD based state machine design – Introduction to FPGA technologies – Algorithms – Nested loop programs and data flow graphs – Design example of pipelined adder – Pipelined FIR filter

UNIT IV FAULT DIAGNOSIS AND TEST GENERATION METHODS 9

Modeling of faults in digital circuits – Temporary faults – Fault diagnosis – Test generation for combinational logic circuits – Path sensation – Boolean difference – D algorithm – PODEM – Detection of multiple faults – Test generation for sequential circuits – Random testing

UNIT V FAULT TOLERANT AND DESIGN FOR TESTABILITY 9

Introduction of fault tolerance – Dynamic redundancy – Hybrid redundancy – Fault tolerant design of memory systems using error correcting codes – Controllability and absorbability – Built in self-test

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Donald Givone, "Digital Principles and Design", 2nd edition ,McGraw Hill Education, 2017
2. Michael D. Ciletti, "Advanced Digital Design with the VERILOG HDL, 2nd edition, Pearson Education, 2011

REFERENCES:

1. Charles H.Roth, "Fundamentals of Logic Design", Thomson Learning, 7th edition, 2013
2. William I. Fletcher, "An Engineering Approach to Digital Design", Pearson Education India, 2015
3. Comer, "Digital Logic and State Machine Design", 3rd edition, Oxford University Press, 2014

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Analyze synchronous sequential networks for digital circuits.	Analyze
CO2	Examine the performance of asynchronous sequential networks	Analyze
CO3	Apply suitable algorithms for FPGA based combinational logic circuits design	Apply
CO4	Summarize different test generation methods for fault diagnosis	Understand
CO5	Explain fault tolerance design of memory systems	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	-	-	2
CO2	3	3	3	-	-	2
CO3	3	2	1	-	-	-
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	2.6	2	1.8	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP04	DESIGN OF SYSTEM ON CHIP	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI design

COURSE OBJECTIVES:

- To learn the fundamental concepts of system design
- To study various processors, synthesis and encoding techniques
- To understand the interconnect architectures and testing in SoC design

UNIT I FUNDAMENTALS TO THE SYSTEM APPROACH 9

System architecture – Components of the system – Hardware and software – Processor architectures – Memory and addressing – System level interconnection – An approach for SoC design – Systemarchitecture and complexity

UNIT II SYSTEM-LEVEL DESIGN 9

Processor Selection for SoC – Concepts in processor architecture and processor micro architecture – Elements in instruction handling – Buffers – Minimizing pipeline delays – Branches – More robust processors – Vector processors and vector instructions extensions – VLIW Processors – Superscalar processors

UNIT III SYNTHESIS AND ENCODING TECHNIQUES 9

Bus topology – Bus protocol architecture – Physical implementation aware – Memory communication architecture – Cache memory – Techniques for power reduction, capacitive crosstalk delay, inductive crosstalk effects – Techniques for fault tolerance and reliability

UNIT IV INTERCONNECT CUSTOMIZATION 9

Interconnect architectures – Bus – Basic architectures – SoC standard buses – Analytic bus models – Using the bus model – Effects of bus transactions and contention time – SoC customization – Customizing instruction processor – Optical interconnects – RF/Wireless interconnects – CNT interconnects

UNIT V SoC IMPLEMENTATION AND TESTING 9

Processor IP – Memory IP – Wrapper design – Real-Time Operating System (RTOS) – Peripheral interface and components – High density FPGAs – EDA tools used for SoC design – Manufacturing test of SoC – Core layer – System layer – Application layer – P1500 wrapper standardization – SoC Test Automation (STAT) – Case studies – High voltage interface controller – SC2A11 multi-core processor

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip", 1st edition WileyIndia Pvt. Ltd, 2011
2. Sudeep Pasricha, Nikil Dutt, "On Chip Communication Architectures: System on ChipInterconnect", 2nd edition, Morgan Kaufmann Publishers, 2008

REFERENCES:

1. Steve Furber, "ARM System on Chip Architecture ", 2nd edition, Addison Wesley Professional,2000
2. Ricardo Reis, "Design of System on a Chip: Devices and Components", 1st edition, Springer, 2004
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification –Methodologies and Techniques", 2nd edition, Kluwer Academic Publishers,2001
4. C.Rowen," Engineering the Complex SOC: Fast, Flexible Design with Configurable Processors,1st edition, Prentice Hall, 2004

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Outline the fundamentals of system on chip	Understand
CO2	Summarize different processors used in system design	Understand
CO3	Illustrate various synthesis and encoding techniques in SoC	Understand
CO4	Identify the appropriate architecture for interconnect customization	Apply
CO5	Analyze the performance of EDA tools in design and testing	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.4	1.6	1.4	-	-	2
Correlation levels:		1: Slight (Low)	2: Moderate (Medium)			3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP05	SCRIPTING LANGUAGE FOR VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Programming Language

COURSE OBJECTIVES:

- To study requirements of software systems for implementing the scripting languages
- To apply PERL and advanced PERL scripting for simple applications
- To understand multi-paradigm systems and high-level general purpose language scripts

UNIT I LINUX ESSENTIALS 9

Introduction to Linux – File system of the Linux – General usage of Linux kernel 7 basic commands – Linux users and group – Permissions for file – Directory and users – Searching a file and directory – Zipping and unzipping concepts – Introduction to shell script

UNIT II FUNDAMENTALS TO SCRIPTS AND PERL LANGUAGE 9

Characteristics and uses of scripting languages – Introduction to PERL – Names and values – Variablesand assignment – Scalar expressions – File handles – Operators – Control structures – Regular expressions – Built-in data types – Statements and declarations – Simple – Compound – Loop statements
– Global and scoped declarations

UNIT III ADVANCED PERL SCRIPTING 9

Finer points of looping – Subroutines – Using pack and unpack – Typeglobs – Eval – References – Data structures – Packages – Libraries and modules – Objects – Tied variables – Interfacing to OS – Creating Internet-aware applications – Dirty hands internet programming – Security issues

UNIT IV TCL RUDIMENTS 9

TCL fundamentals – String and pattern matching – Structure Syntax – Parser – Variables and data in TCL control flow – Data structures – Simple input/output – Procedures and scope – Libraries and packages – Namespaces – Making applications internet aware – Nuts and bolts internet programming

UNIT V AUXILIARY LANGUAGES 9

JavaScript – Object models – Design philosophy – Versions of JavaScript – The Java script core language – Introduction to Python – Using the Python interpreter – More control flow tools – Data structures – Modules input and output – Errors and exceptions – Classes – Brief tour of the standard library

Contact Periods:

Lecture : 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. David Barron, "The World of Scripting Languages", 1st edition, Wiley Publication, 2000
2. Randal L, Schwartz Tom Phoenix, "Learning PERL", 3rd edition, O'Reilly Publications, 2001

REFERENCES:

1. Tom Christiansen, Brian D Foy, Larry Wall, and John Orwant, "Programming PERL", 4th edition,O'Reilly Media, Inc. Publishers, 2012
2. M.Lutz,SPD, "Programming Python", 4th edition, O'Reilly Media, Inc. Publishers, 2010
3. Steve Holden and David Beazley, "Python Web Programming", 1st edition, New RidersPublications, 2002
4. J.Lee and B.Ware ,"Open Source Web Development with LAMP using Linux Apache, MySQL,Perl and PHP", 1st edition, Addison Wesley Professional Publisher, 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain basic commands of Linux to work in Linux environment	Understand
CO2	Illustrate elementary commands of PERL in system design	Understand
CO3	Examine the scripts involved in advanced PERL language	Analyze
CO4	Make use of scripts to run in TCL environment	Apply
CO5	Summarize the basics of JAVA and PYTHON scripts	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	3	3	-	-	2
CO4	3	2	1	-	-	-
CO5	2	1	1	-	-	-
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP06	SYSTEM VERILOG	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Verilog Programming

COURSE OBJECTIVES:

- To understand the basic concepts of System Verilog
- To learn different statements and interfaces of System Verilog
- To apply System Verilog programming for real time application

UNIT I BASICS OF SYSTEM VERILOG 9

Introduction to System Verilog – Packages – Declarations – Simulation time units – Precision –Variables – Data types

UNIT II DATA STRUCTURES 9

Structures – Declarations – Packed structures – Passing structures – Unions – Packed, unpacked,tagged Unions – Arrays – Array operation

UNIT III STATEMENTS AND CONTROL STRUCTURES 9

Procedural blocks – Combinational, sequential and latched logic – Enhancements to tasks and functions – Operand enhancements – New jump statements – Enhanced case statements – Enhanced if else decision

UNIT IV SYSTEM VERILOG DESIGN VERIFICATION 9

Verification method implementation – Response checking – Assertions – Internal DUT signals –External interfaces – Reusable assertions based checkers

UNIT V HARDWARE SECURITY 9

Reasons for raise of hardware security issues – IC Counterfeiting – IP piracy – Hardware trojans – Debug security and applications of Physical Unclonable Functions (PUF)

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Simon Davidmann,"System Verilog for Design",2nd edition,2003
2. Tehranipoor, Mohammad, Wang, Cliff, "Introduction to Hardware Security and Trust Editors", 3rd edition Springer, 2012

REFERENCES:

1. Janick Bergeron, "Writing Test Benches Functional Verification of HDL Models",3rd edition,Springer, 2003
2. Andreas Meyer, "Principles of Functional Verification", 5th edition, Newness, 2003
3. Chris Spear, "System Verilog for Verification: A Guide to Learning the Test benchLanguage Features", 5th edition, Springer, 2008
4. T.Kropf, "Introduction to Formal Hardware Verification", 7th edition, Springer Verlag, 2010

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the basic concepts of System Verilog	Understand
CO2	Illustrate the operations of data structures	Understand
CO3	Make use of procedural statements in system Verilog programming	Apply
CO4	Summarize different verification process in system Verilog	Understand
CO5	Analyze security issues in hardware using system Verilog	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP07	DESIGN OF SEMICONDUCTOR MEMORIES	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design

COURSE OBJECTIVES:

- To study the concepts of volatile and non-volatile memory architectures
- To analyze various testing methods of semiconductor memories
- To understand the advanced semiconductor memory packaging technologies

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES 9

SRAM cell structures – MOS SRAM architectures – MOS SRAM cell – Bipolar SRAM technologies – Silicon On Insulator (SOI) technology – Advanced SRAM architectures and technologies – DRAM technology development – CMOS DRAMs – DRAMs cell theory – Bi-CMOS – DRAMs – Soft errorfailures in DRAMs – Advanced DRAM designs and architectures

UNIT II NON-VOLATILE MEMORIES 9

Masked Read-Only Memories - High density ROMs – Programmable Read-Only Memories – Bipolar PROMs – CMOS PROMs – EPROMs – Floating-Gate EPROM Cell – One-Time Programmable EEPROMs – EEPROM technology and architectures – Non-Volatile SRAM – Flash memories (EPROMs or EEPROM) – Advanced flash memory architectures

UNIT III MEMORY FAULT MODELING AND TESTING 9

RAM fault modeling – Electrical testing – Pseudo random testing – Megabit DRAM testing non-volatile memory modeling and testing – IDDQ fault modeling and testing – Application specific memory testing

UNIT IV SEMICONDUCTOR RADIATION EFFECTS 9

Radiation effects – Single event phenomenon – Radiation hardening techniques – Radiation hardening process and design issues – Radiation hardened memory characteristics – Radiation hardness assurance and testing – Radiation dosimetry – Water level radiation testing and test structures

UNIT V ADVANCED MEMORY TECHNOLOGIES 9

Introduction to memory technologies – High-density memory packing technologies – Gallium Arsenide (GaAs) FRAMs – Analog memories – Magneto resistive random access memories – Experimental memory devices – Ferroelectric random access memories – Memory hybrids and MCMs (2D) - Memory stacks and MCMs (3D)

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Ashok.K.Sharma, "Semiconductor Memories: Technology, Testing and Reliability", Wiley IEEEpress, New York, 2nd Edition,2010
2. Brent Keeth, R. Jacob Baker, Brian Johnson, Freng Lin, "DRAM Circuit Design: Fundamental and High Speed Topics", Wiley-IEEE Press, 2nd edition, 2012

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REFERENCES:

1. Ashok K. Sharma, "Semiconductor Memories", Two-Volume Set, Wiley-IEEE Press, 2003
2. Betty Prince, "High Performance Memories: New Architecture DRAMs and SRAMs – Evolutionand Function", Wiley, Revised Edition, 1999
3. Sharma, Ashok K., "Semiconductor Memories: Technology, Testing, and Reliability", Wiley- IEEE Press, New York, 2002
4. Tegze P. Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers, 2nd edition, 2007

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Illustrate the micro level operations of Random Access Memories	Understand
CO2	Compare the performance of various non-volatile memories	Analyze
CO3	Identify the suitable fault modeling technique for memory testing	Apply
CO4	Outline the radiation effects of memory	Understand
CO5	Summarize the concepts of advanced memory technologies	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	2	1	-	-	-
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP08	TESTING OF VLSI CIRCUITS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital design

COURSE OBJECTIVES:

- To understand the basics of simulation techniques and test generation
- To learn the different test methods for single struck at faults
- To familiarize the concept of built-in self-test and design for testability

UNIT I FAULT SIMULATION 9

Introduction to testing – Faults in digital circuits – Modeling of faults – Logical fault models – Fault detection – Fault location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate level event–driven simulation

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits – Truth table and fault matrix-path sensitization – D algorithm – PODEM – FAN – Delay fault detection – Testing of sequential circuits – Designing and checking experiments – Test generation using the circuit structure and the state table

UNIT III TESTING FOR SINGLE STRUCK-AT-FAULTS 9

ATG in combinational circuits – Fault oriented ATG – Fault independent ATG – Random test generation – ATG in sequential circuits – TG using iterative array models – Simulation based TG – TG using RTL models – Random test generation

UNIT IV BUILT IN SELF-TEST 9

Built-in self-test – Test pattern generation for BIST – Circular BIST – BIST architecture – Testable memory design – Test algorithms – Test generation for embedded RAMs

UNIT V DESIGN FOR TESTABILITY 9

Adhoc design for testability techniques – Controllability and observability – Storage cells for scan designs – Level Sensitive Scan Design (LSSD) – Partial scan – Boundary scan

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Abramovici .M, Breuer M.A and Friedman A.D, "Digital Systems and Testable Design", 2nd edition,Jaico Publishing House, 2002
2. Bushnell M.L and Agrawal V.D, "Essentials of Electronic Testing for Digital Memory and Mixed–Signal VLSI Circuits", 1st edition, Kluwer Academic Publishers, 2004

REFERENCES:

1. Z.Navabi, Digital System Test and Testable Design, Springer, 2011
2. Lala P.K, "An Introduction to Logic Circuit testing",1st edition, Morgan & Claypool Publishers, 2007
3. Parag K. Lala, "Self–checking and fault tolerant digital design", 1st edition, Morgan Kaufmann, 2006
4. Xiaoqing Wen, Cheng Wen Wu and Laung Terng Wang, "VLSI Test Principles and Architectures: Design for Testability", 1st edition, Cambridge University Press, 2006

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize the concepts of fault simulation and fault diagnosis	Understand
CO2	Interpret the test generation for combinational and sequential circuits	Understand
CO3	Examine different testing methods for single struck at faults	Analyze
CO4	Illustrate various BIST architecture and different test algorithms	Understand
CO5	Test for fault identification using DFT approach	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	3	3	-	-	2
CO4	2	1	1	-	-	-
CO5	3	2	1	-	-	-
CO	2.4	1.6	1.4	-	-	2
Correlation levels:		1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP09	INTERCONNECTIONS AND PACKAGING FOR VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design

COURSE OBJECTIVES:

- To study the interconnections and its applications
- To understand the parameters associated with interconnects
- To learn the IC Manufacturing and packaging process

UNIT I INTRODUCTION TO INTERCONNECTIONS 9

Interconnections for VLSI Applications – Metallic,Optical and Superconducting interconnections – Copper interconnections – Methods of images and moments – Capacitance – Transmission line equations – Millers theorem

UNIT II INTERCONNECTION PARAMETERS 9

Parasitic resistance – Parasitic capacitance – Parasitic inductance – Green function matrix – Printing and embedding on substrate – Interconnection delays – Compact expressions and delay in multilayer integrated circuits

UNIT III FUTURE INTERCONNECTIONS 9

Optical interconnections – Transmission line models – Super conducting interconnections – Nano technology circuit interconnections

UNIT IV IC MANUFACTURING TECHNOLOGIES 9

Overview of manufacturing process – Environment – Photolithography – Methodology and packaging – Assembly and interconnection – Manufacturing technologies

UNIT V PACKAGING THE IC 9

Single chip packaging – Trends in IC Packaging – Area array packages – Multi chip packaging – System in Package(SiP) – System on Package (SoP) – Known Good Die (KGD) – Chip on board

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1 Ashok K Goel, "High–Speed VLSI Interconnections", 2nd edition, Wiley–Interscience, IEEE Press,2015
2 Hartmut Grabinski, "Interconnects in VLSI Design", 1st edition, Springer Science, 2000

REFERENCES:

1 William Greig, "Integrated Circuit Packaging: Assembly and Interconnections", 1st edition,Springer Series in Advanced Microelectronics, 2010
2 Francesc Moll and Miquel Roca, "Interconnection noise in VLSI Circuits", 1st edition, Kluwar Academic Publishers, 2012
3 H. B. Bakoglu, "Circuits, Interconnections, and Packaging for VLSI", 1st edition, Addison Wesley Longman, 1990

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize the different types of interconnections and its applications	Understand
CO2	Examine the performance of various parameters associated with interconnections	Analyze
CO3	Identify the appropriate future interconnections for VLSI circuits	Apply
CO4	Explain the types of IC Manufacturing technologies	Understand
CO5	Illustrate the single chip and multichip packaging of VLSI system	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	2	1	-	-	-
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	2.4	1.6	1.4	-	-	2
Correlation levels:		1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP10	VLSI SIGNAL PROCESSING	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital Signal Processing

COURSE OBJECTIVES:

- To learn various methods for critical path reduction
- To design digital filters and arithmetic architectures
- To understand pipelining concepts in digital filters

UNIT I METHODS OF CRITICAL PATH REDUCTION 9

Introduction to digital signal processing systems – Typical DSP algorithms – Iteration bound – Retiming – Properties and techniques – Unfolding – Folding

UNIT II CONVOLUTION AND ALGORITHMIC STRENGTH REDUCTION METHODS 9

Fast convolution – Cook toom – Winograd algorithm – Parallel FIR filters – Discrete cosine transform and inverse DCT – Parallel architecture for rank order filters

UNIT III DESIGN OF DIGITAL FILTERS 9

Scaling and round off noise computation in digital filters – Schur algorithm – Digital basic lattice filters – One multiplier lattice filter – Normalized lattice filter – Roundoff noise calculation in lattice filters

UNIT IV DESIGN OF ARITHMETIC ARCHITECTURES 9

Bit level arithmetic architectures – Parallel multipliers – Bit serial multipliers – Redundant number representations – Radix-2 hybrid redundant multiplication architectures

UNIT V PIPELINING CONCEPTS 9

Introduction to Pipelining and parallel processing – Synchronous pipelining and clock styles – Clock skew and clock distribution – Wave pipelining – Implementation of wave pipelined systems –Asynchronous pipelining

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Keshab K.Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", JohnWiley, Indian Reprint, 2007
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, 2nd edition, Indian Reprint, 2014

REFERENCES:

1. J. G. Chung and Keshab K. Parhi, "Pipelined Lattice and Wave Digital Recursive Filters", SpringerPublisher, 1996
2. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw-Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall,1985
4. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunicationand Signal Processing", Prentice Hall, 1994

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize various critical path reduction techniques	Understand
CO2	Construct pipelined and parallel FIR filters	Apply
CO3	Classify the various digital lattice filter	Understand
CO4	Illustrate bit level and redundant arithmetic architectures	Understand
CO5	Compare various synchronous and asynchronous pipelining concepts	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	2	1	-	-	-
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.4	1.6	1.4	-	-	2
Correlation levels:		1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP11	QUANTUM COMPUTING	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Electronic Devices and Circuits

COURSE OBJECTIVES:

- To understand the fundamentals of quantum information processing
- To learn the quantum computation principles and algorithms
- To study the computing performance and models for quantum computing

UNIT I QUANTUM MEASUREMENTS 9

Introduction – Quantum measurements density matrices – Positive – Operator valued measure – Fragility of quantum information – Decoherence – Quantum superposition and entanglement –Quantum gates and circuits

UNIT II QUANTUM BASICS AND PRINCIPLES 9

Quantum basics and principles – No cloning theorem and quantum teleportation – Bell's inequality and its implications – Quantum algorithms and circuits

UNIT III ALGORITHMS 9

Algorithms – Deutsch and deutsch – Jozsa algorithms – Grover's search algorithm – Quantum fourier transform – Shore's factorization algorithm

UNIT IV PERFORMANCE, SECURITY AND SCALABILITY 9

Performance – Security and scalability – Quantum error correction – Fault tolerance – Quantum cryptography – Implementing quantum computing – Issues of fidelity – Scalability in quantum computing

UNIT V QUANTUM COMPUTING MODELS 9

Quantum computing models – NMR quantum computing – Spintronics and QED MODEL – Linear optical model – Nonlinear optical approaches – Limits of all the discussed approaches – Future of quantum computing

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Eric R. Johnston, Nic Harrigan, "Programming Quantum Computers: Essential Algorithms and Code Samples", 1st edition, 2019
2. Dr. Christine Corbett Moran, "Mastering Quantum Computing with IBM QX: Explore the world of quantum computing using the Quantum Composer and Qiskit", 1st edition, 2019

REFERENCES:

1. V.K Sahni, "Quantum Computing (with CD)", 1st edition, TATA McGrawHill, 2022
2. Chris Bernhardt, "Quantum Computing for Everyone", 1st edition, The MIT Press, 2020
3. Riley Tipton Perry, "Quantum Computing from the Ground Up", 1st edition, World Scientific Publishing Ltd, 2012
4. Michael A. Nielsen and Issac L. Chuang, "Quantum Computation and Information", 1st edition, Cambridge 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize the basic quantum measurements	Understand
CO2	Explain the principles of basic quantum systems	Understand
CO3	Implement suitable quantum algorithms for quantum circuits	Apply
CO4	Illustrate the concepts of security and scalability	Understand
CO5	Analyze the performance of different quantum computing models	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	2	1	-	-	-
CO	2.4	1.6	1.4	-	-	2
Correlation levels:		1: Slight (Low)	2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP12	VLSI FOR WIRELESS COMMUNICATION	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design Techniques
- Digital Communication

COURSE OBJECTIVES:

- To learn the fundamentals of communication systems
- To study transmitter and receiver architectures of VLSI for wireless communication
- To understand frequency synthesizer and types of mixers

UNIT I FUNDAMENTALS OF COMMUNICATION SYSTEMS AND LNA 9

Overview of wireless systems – Access methods – Modulation schemes – Classical channels – Wireless channel description – Path loss – Multipath fading – Low noise amplifier – Wideband LNA design – Narrow band LNA – Impedance matching – Core amplifier

UNIT II TRANSMITTER ARCHITECTURES 9

Transmitter back end – Design philosophy – Direct conversion and other architectures – Quadrature LO generator – Single ended RC – Single ended LC – RC with differential stages – Divider based generator – Power amplifier design – Specs, Power output control, PA design issue Class A, AB, B, C, E amplifiers

UNIT III MIXERS 9

Balancing Mixer – Gilbert Mixer – Conversion Gain – Distortion - A Complete Active Mixer - Switching Mixer - Unbalanced switching mixer - Conversion gain – Distortion – Sampling Mixer – Single ended sampling mixer – Conversion gain, distortion, intrinsic noise and extrinsic noise

UNIT IV FREQUENCY SYNTHESIZER 9

PLL based frequency synthesizer – Phase detector – Dividers – LC oscillators – Ring oscillators – Phase noise – A Complete synthesizer design example (DECT application) – Loop filter – First order – Second order and High order filters

UNIT V RECEIVER ARCHITECTURES 9

Receiver front end – General design philosophy – Heterodyne and other architectures – Filter design – Band Selection Filter (BPF1), Image Rejection Filter (BPF2) and Channel Filter (BPF3) – Nonidealities and design parameters – Nonlinearity noise derivation of NF, IIP3 of receiver front end

Contact Periods:

Lecture: 45 Periods Tutorial: - Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Bosco H Leung "VLSI for Wireless Communication", 4th edition, Pearson Education, 2002
2. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", 1st edition, Kluwer Academic Publishers, 2000

REFERENCES:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd edition, McGraw –Hill, 1999
2. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, 1st edition, Kluwer Academic Publications, 1997
3. Thomas H.Lee, "The Design of CMOS Radio–Frequency Integrated Circuits", 1st edition, Cambridge University Press, 2003.
4. B. Razavi," RF Microelectronics", 2nd edition, Prentice-Hall, 1998

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Outline the fundamentals of communication system	Understand
CO2	Explain different modules in transmitter architectures	Understand
CO3	Make use of active and passive mixer for VLSI circuits	Apply
CO4	Analyze different phase and frequency processing components	Analyze
CO5	Illustrate the various receiver architectures	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	1	-	-	-
CO4	3	3	3	-	-	2
CO5	2	1	1	-	-	-
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP13	ADVANCED EMBEDDED SYSTEM	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Embedded Systems

COURSE OBJECTIVES:

- To study the architecture and assembly language programming of ARM processor
- To learn the data types and memory hierarchy
- To understand the architectural support for system development and embedded ARM applications

UNIT I ARM ARCHITECTURE 9

Processor architecture and organization – Abstraction in hardware design – RISC Instruction set – THUMB register – Stack instructions – Acorn RISC machine – Architecture inheritance – ARM programmer's model – ARM development tools – ARM instruction execution and implementation – ARM co-processor interface

UNIT II ARM ASSEMBLY LANGUAGE PROGRAMMING 9

Data processing instructions – Data transfer instructions – Control flow instructions – The ARM instruction set – Coprocessor instructions – Memory faults – ARM architecture variants

UNIT III ARCHITECTURAL SUPPORT FOR HIGH-LEVEL LANGUAGES 9

Abstraction in software design – Data types – Floating-point data types – The ARM floating-point architecture – Conditional statements – Functions and procedures – Use of memory – Memory hierarchy

UNIT IV ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT 9

ARM memory interface – Advanced microcontroller bus architecture – Hardware system prototyping tools – ARM debug architecture – Embedded trace – Signal processing support – ARM processor cores

UNIT V EMBEDDED ARM APPLICATIONS 9

VLSI Ruby II advanced communication processor – ISDN subscriber processor – Bluetooth baseband controller – ARM7500 and ARM7500FE – ARM7100 – SA 1100

Contact Periods:

Lecture: 45 Periods Tutorial: –Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Steve B Furber, "ARM System on Chip Architecture", 2nd edition, Pearson Education, 2015
2. Ata Elahi and Trevor Arjeski, "ARM Assembly Language with Hardware Experiments",1st edition, Springer, 2014.

REFERENCES:

1. Muhammad Ali Mazidi and Sarmad Naimi, "ARM Assembly Language Programming and Architecture '2nd edition, Microdigital education, 2019
2. Ricardo Reis and Jochen A.G, "Design of System on a Chip: Devices and Components", 1st edition, Springer, 2004
3. William Hohl and Christopher Hinds, "ARM Assembly Language: Fundamentals and Techniques", 2nd edition, CRC Press, 2014
4. Bob Zeidman, "Designing with FPGAs and CPLDs", 4th edition, Elsevier, CMP Books, 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Interpret different types of ARM architectures	Understand
CO2	Choose the appropriate instructions for assembly language programming	Apply
CO3	Infer the high - level language and memory hierarchy	Understand
CO4	Explain the architectural support for system development	Understand
CO5	Examine the performance of ARM in embedded applications	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	2	1	-	-	-
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.4	1.6	1.4	-	-	2
Correlation levels:		1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP14	INDUSTRIAL INTERNET OF THINGS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Real time Embedded Systems

COURSE OBJECTIVES:

- To learn fundamentals of Internet of Things (IoT)
- To understand the IoT protocol standards and design methodologies
- To apply the concepts of IoT in real-time applications

UNIT I PHYSICAL DESIGN OF IoT 9

Things in IoT – IoT Protocols – Functional blocks – Communication models – Communication APIs – IoT enabling technologies – IoT levels and deployment templates – Domain specific IoTs

UNIT II IoT ARCHITECTURE 9

M2M high level ETSI architecture – IETF architecture – OGC architecture – IoT reference model – Domain model – Information model – Functional model – Communication model – IoT reference architecture

UNIT III IoT DESIGN METHODOLOGY AND PROTOCOLS 9

Purpose and requirements specification – Process specification – Domain and information model specification – Application development – Protocol standardization for IoT – M2M and WSN protocols – SCADA and RFID protocols – Zigbee architecture – Network layer – 6LowPAN – CoAP – Security

UNIT IV LOGICAL DESIGN USING PYTHON 9

Python data types and data structures – Control flow – Functions – Classes – Python packages of interest for IoT – Raspberry Pi interfaces – Programming raspberry Pi with python

UNIT V CASE STUDIES 9

Home intrusion detection – Smart parking – Weather reporting bot – Forest fire detection – Smart irrigation – IoT printer – Data analytics for IoT – Management tools for IoT cloud storage models, communication APIs – Cloud for IoT

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A hands–on approach", 1st edition, Universities Press, 2015
2. Olivier Hersent, David Boswarthick, Omar Elloumi, "The Internet of Things –Key applications and Protocols", 1st edition, Wiley, 2015

REFERENCES:

1. Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", 1st edition, CRC Press, 2012
2. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand, David Boyle, "From Machine–to–Machine to the Internet of Things – Introduction to a New Age of Intelligence", 1st edition, Elsevier, 2014
3. Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds), "Architecting the Internet of Things", Springer, 2011

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4. Hanes David , Salgueiro Gonzalo, Grossetete Patrick, Barton Rob, Henry Jerome, "IoT Fundamentals: Networking Technologies, Protocols and Use Cases for the Internet of Things", 1st edition, Pearson Education, 2017

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Illustrate the basics of Internet of Things and its levels	Understand
CO2	Infer different IoT architecture design related to real-time applications	Understand
CO3	Interpret the different IoT communication protocols	Understand
CO4	Examine the performance of various Raspberry Pi interfaces for simple applications	Analyze
CO5	Solve a real-world problem using the concept of Industrial Internet ofThings	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	3	3	-	-	2
CO5	3	2	1	-	-	1
CO	2.4	1.6	1.4	-	-	1.5
Correlation levels:		1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP15	SECURITY SOLUTIONS IN VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Network Security

COURSE OBJECTIVES:

- To understand the different kinds of threats in VLSI
- To acquaint knowledge about security counter measure and reconfigurable computing
- To study various hardware-based security challenges and solutions

UNIT I FUNDAMENTALS OF SECURITY 9

Security attacks – Security services – Security mechanisms – Security model – Threats to security – Physical security – Biometric systems – Monitoring controls – Data security – Computer system security – Communication security

UNIT II SECURITY COUNTER MEASURES 9

Cryptography in network security – Network encryption – Browser encryption – Onion routing – IP security protocol suite – Virtual private networks – System architecture – Firewalls – Types of firewalls – Personal firewalls – Comparison of firewall types – Network address translation

UNIT III RECONFIGURABLE COMPUTING 9

Reconfigurable computing system – PAM – VCC – Splash – PRISM – Teramac – Cray – SRC – Non- FPGA – Reconfiguration management – Reconfiguration – Configuration architectures – Managing reconfiguration process – Reducing reconfiguration time – Configuration security

UNIT IV SECURITY CHALLENGES IN VLSI 9

Recent security issues – Case study – Testability issues in modern VLSI – Superscalar architecture – Intel pentium processor – Hardware security challenges beyond CMOS – Wireless network security – Security information and event management

UNIT V CRYPTO CHIP DESIGN AND HARDWARE SECURITY 9

VLSI implementation of AES algorithm – Implementation of DES – Development of digital signature chip using RSA algorithm – Hardware based security solution – Hardware accelerators – Security enhancement techniques – Hardware trojans

Contact Periods:

Lecture: 45 Periods Tutorial: - Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Charels P. P fleeger "Security in Computing", 1st edition, PHI, 2006
2. Wayne wolf, "Modern VLSI Design: IP-based Design", 4th edition, Pearson Education,2009

REFERENCES:

1. Bobda Christophe, "Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications", 1st edition, Springer, 2007
2. Hauck Scott, Dehon A, "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation", 1st edition, Elsevier, 2007
3. William Stalling "Cryptography and Network Security", 4th edition, Pearson Education, 2005
4. Jeff Crume "Inside Internet Security", 1st edition, Addison Wesley, 2000

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the basic concept of security mechanism	Understand
CO2	Examine the different security prevention methods	Analyze
CO3	Make use of reconfigurable system in recent application domains	Apply
CO4	Infer the security challenges in modern VLSI	Understand
CO5	Choose the appropriate cryptography algorithms for hardware security.	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	2	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	2	1	-	-	-
CO	2.6	1.8	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP16	THERMAL ANALYSIS OF INTEGRATED CIRCUITS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Nil

COURSE OBJECTIVES:

- To understand about thermal issues in CMOS
- To learn testing and modeling of IC for thermal conditions
- To study the basics behind characteristics and thermal designing of VLSI circuits

UNIT I THERMAL ISSUES IN VLSI CIRCUITS 9

Evolution of CMOS technology – Emergence of thermal issues – Power in nanometer regime – Leakage reduction techniques – Junction temperature projections for deep sub-micron technologies – Reliability issues in scaled technologies

UNIT II TESTING ICs FOR NORMAL OPERATING CONDITIONS 9

Burn-in test – Temperature and voltage acceleration factors – Technology scaling and burn-in – Burn-in elimination – Estimation of junction temperature increase with technology scaling under burn-in conditions – Packaging considerations for burn-in – Cooling techniques for burn-in – Burn-in limitations and optimization

UNIT III THERMAL AND ELECTRO THERMAL MODELING 9

Objectives of thermal analysis – Thermal network modeling – Architectural level electro thermal modeling – Electro thermal modeling at logic level – Circuit level – Device level

UNIT IV THERMAL RUNAWAY AND THERMAL MANAGEMENT 9

Thermal awareness – Thermal runaway – Thermal runaway during burn-in-thermal management – During normal operating conditions – Temperature management: a case study – Temperature measurement of semiconductor devices

UNIT V LOW TEMPERATURE CMOS OPERATION 9

Low temperature motivation – Low temperature characterization of CMOS devices – Reliability at low temperature – Microprocessor low temperature operation – A Case Study – Disadvantages of low temperature electronic cooling – Cooling

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Yi-Kan Cheng, Ching-Han Tsai, Chin-Chi Teng and Sung-Mo Kang, , "Electro Thermal Analysisof VLSI Systems", 3rd edition, Kluwer Academic Publishers, 2002
2. Arman Vassighi and Manoj Sachdev, "Thermal and Power Management of Integrated Circuits",2nd edition, Springer, 2006

REFERENCES:

1. Mona M. Hella, Patrick Mercier, "Power management Integrated Circuits", 1st edition, CRC Press,2018
2. Phillip E. Allan, Douglas R. Holberg, "CMOS Analog Circuit Design", 2nd edition, Oxford UniversityPress, 2002
3. N.K. Jha, Sandeep Gupta, "Testing of Digital Systems", 4th edition, Cambridge University Press,2012
4. William Stalling "Cryptography and Network Security", 4th edition, Pearson Education, 2005

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain various thermal issues of VLSI circuits	Understand
CO2	Examine the IC operation through testing under various conditions	Analyze
CO3	Analyze the thermal and electro thermal modeling at different levels	Analyze
CO4	Identify thermal runaway problems of semiconductor devices	Apply
CO5	Summarize different CMOS operations at low temperature	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	3	3	-	-	2
CO4	3	2	1	-	-	-
CO5	2	1	1	-	-	-
CO	2.6	2	1.8	-	-	2
Correlation levels:		1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP17	OPTIMIZATION ALGORITHM FOR VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Nil

COURSE OBJECTIVES:

- To learn the methods of optimization
- To study optimization algorithm based on neural networks, fuzzy and genetic algorithms
- To understand implementation of particle swarm optimization

UNIT I NATURE INSPIRED ALGORITHMS 9

Introduction to algorithm – Newton's method – Optimization algorithm – No-free-lunch theorems –Nature – Inspired meta heuristics – Analysis of algorithms – Parameter tuning and parameter control

UNIT II NEURAL NETWORKS AND FUZZY LOGIC SYSTEMS 9

Neural network – Back propagation network, Generalized delta rule – Radial basis function network– Interpolation and approximation RBFNS – Comparison between RBFN and BPN – Basic of fuzzy logictheory – Crisp and fuzzy sets – Basic set operation – Neuro-Fuzzy modelling – Adaptive Neuro – Fuzzy Inference System (ANFIS) – ANFIS architecture – Hybrid learning algorithm

UNIT III EVOLUTIONARY COMPUTATION AND GENETIC ALGORITHMS 9

Evolutionary Computation (EC) – Features of EC, classification of EC, advantages and applications– Introduction of genetic algorithms – Biological background – Classification of GA

UNIT IV FUNDAMENTALS OF GENETIC ALGORITHM (GA) 9

Terminologies – Genetic algorithms – Mathematical foundations – Computer implementation of GA– Applications of GA – Advanced operators and techniques in genetic research – Introduction to genetic based machine learning – Applications of genetics-based machine learning

UNIT V PARTICLE SWARM OPTIMIZATION 9

Introduction – Principles of bird flocking and fish schooling – Evolution of PSO – Operating principles – PSO algorithm – Neighbourhood topologies – Convergence criteria – Applications of PSO – Honeybee social foraging algorithms – Bacterial foraging optimization algorithm

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Eiben, A.E. Smith and James E, "Introduction to Evolutionary Computing", 2nd edition, Springer2015
2. David E Goldberg, "Genetic algorithms in search, optimization and machine learning", Addison-Wesley, Longman Publishing Co., Inc. Boston, MA, USA, 2009

REFERENCES:

1. Christopher M. Bishop, "Neural Networks for Pattern Recognition", 1st edition, Oxford UniversityPress 1995
2. Bhuvaneswari M.C, "Application of Evolutionary Algorithms for Multi–objective Optimizationin VLSI and Embedded Systems",1st edition, Springer 2015
3. Nello Cristianini, John Shawe, Taylor, "An Introduction to Support Vector Machines and Other Kernel– based Learning Methods", 2nd edition, Cambridge University Press 2013
4. Pakize Erdogmus "Particle Swarm Optimization with Applications",1st edition, Duzce University,Intech 2018

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain the basic concept of optimization algorithm	Understand
CO2	Compare the neural networks and fuzzy logic optimization algorithms	Analyze
CO3	Illustrate the basic concept of evolutionary computation and genetic algorithms	Understand
CO4	Interpret the basic concept of genetic algorithms	Understand
CO5	Examine the performance of Particle Swarm Optimization algorithms	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	2	1	-	-	-
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP18	MEMS AND NEMS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design

COURSE OBJECTIVES

- To understand the fabrication of microsystems and its electrical and mechanical concepts
- To learn the fundamentals of micro-sensors and system issues of micro circuit
- To understand the concept of classical and quantum mechanics

UNIT I INTRODUCTION TO MEMS AND NEMS 9

Introduction – Design of MEMS and NEMS – History of MEMS Development – Intrinsic characteristics of MEMS – Pattern transfer with subtractive techniques – Pattern transfer with additive techniques

UNIT II BASICS OF MICRO FABRICATION 9

Overview – Wafer level process – Substrates – Wafer cleaning – Oxidation of silicon – Local oxidation – Doping – Thin-film deposition – Wafer bonding pattern transfer – Optical lithography – Design rules – Mask making – Wet etching – Dry etching – Additive process – Planarization

UNIT III ELECTRICAL AND MECHANICAL CONCEPTS 9

Conductivity of semiconductors – Crystal planes and orientations – Stress and strain – Flexural beam bending analysis using simple loading conditions – Torsional deflection – Intrinsic stress – Dynamic system – Resonance frequency – Quality factor – Active tuning of spring constant and resonant frequency

UNIT IV ELECTRO STATIC SENSING AND ACTUATION 9

Introduction to electrostatic sensors and actuators – Parallel-plate capacitor – Application of parallel plate capacitors – Interdigitated finger capacitors – Application of comb drive devices

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9

Principle of superposition – Dynamical variables and observables – Representations – Quantum conditions Schrodinger equation – Equations of motion – Elementary applications

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOK

1. Chang Liu, "Foundations of MEMS", 2nd edition, Pearson India, 2016
2. Cornelius T. Leondes, "MEMS/NEMS Handbook– Techniques and Applications", 2nd edition, Springer Publication, 2006

REFERENCES

1. Marc J. Madou, "Fundamentals of Microfabrication and Nanotechnology", 3rd edition, Taylor & Francis, 2011
2. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002
3. A.M. Dirac," Principles of Quantum Mechanics", Oxford University Press, Oxford, 1978
4. Zhuoqing Yang, "Advanced MEMS/NEMS Fabrication and Sensor" Springer, 2021

COURSE OUTCOMES

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain the fundamentals of MEMS and NEMS	Understand
CO2	Summarize the different processes in fabrication of MEMS	Understand
CO3	Interpret the electrical and mechanical concepts of MEMS	Understand
CO4	Make use of actuation techniques in designing MEMS capacitors	Apply
CO5	Distinguish between classical and quantum mechanics	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	1	-	-	1
CO5	2	1	1	-	-	-
CO	2.2	1.2	1	-	-	1
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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PROFESSIONAL ELECTIVE

P23VLP19	MIXED SIGNAL VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Analog Electronics
- Linear integrated circuits

COURSE OBJECTIVES

- To study the mixed signal concepts of submicron CMOS circuits and Integrator based filters.
- To learn the data converters architecture, modelling and signal to noise ratio
- To understand the principle of CMOS integrated circuits based oscillators and PLLs

UNIT I SUBMICRON CMOS CIRCUIT DESIGN 9

Submicron CMOS – Overview and models – CMOS process flow – Capacitors and resistors – Digital circuit design – The MOSFET switch – Delay elements – An adder – Analog circuit design – Biasing – Op-Amp design – Circuit Noise

UNIT II INTEGRATOR BASED CMOS FILTERS 9

Integrator building blocks – Low pass filter – Active RC integrators – MOSFET-C integrators gm – C integrators – Discrete time integrators – Filtering topologies – The bilinear transfer function – The biquadratic transfer function – Filters using noise shaping

UNIT III DATA CONVERTER ARCHITECTURES 9

DAC architectures – Resistor string – R-2R ladder networks – Current steering – Charge scaling DACs – Cyclic DA and Pipeline DAC – ADC architectures – Flash – Two-step flash ADC – Pipeline ADC – Integrating ADC's – Successive approximation ADC

UNIT IV DATA CONVERTER MODELING AND SNR 9

Sampling and aliasing – A modeling approach – Impulse sampling – The sample and hold – Quantization noise – Data converter SNR – An overview – Clock Jitter – Improving SNR using averaging – Decimating filter for ADCs – Interpolating filter for DACs – Band pass and high pass sinc filters – SNR improvement

UNIT V OSCILLATORS AND PLL 9

LC oscillators – Voltage controlled oscillators – Simple PLL – Charge pumps PLLs – Non-ideal effects in PLLs – Delay locked loops

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits by Behzad Razavi, McGraw Hill, 33rd Re- print, 2016
2. CMOS Mixed Signal Circuit Design by R.Jacob Baker, Wiley India, IEEE Press, reprint 2008

REFERENCES:

1. CMOS Circuit Design, Layout and Simulation by R.Jacob Baker, Wiley India, IEEE Press, Second Edition, reprint 2009.Phillip E.Allen and Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002
2. Tony Chan Carusone, David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2nd Edition, 2011
3. R.J. Baker, "CMOS Mixed-Signal Circuit Design", Wiley Publications, 2002

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KPRIET
Learn Beyond

COURSE OUTCOMES

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain the fundamental concepts for mixed signal CMOS circuits.	Understand
CO2	Illustrate the characteristics of IC based CMOS filters.	Understand
CO3	Summarize the various data converter architectures.	Understand
CO4	Select the appropriate methods to improve the SNR in data converters.	Apply
CO5	Design oscillators and phase lock loop circuit for given specifications.	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	1	-	-	1
CO5	2	1	1	-	-	-
CO	2.2	1.2	1	-	-	1
Correlation levels:		1: Slight (Low)	2: Moderate (Medium)			3: Substantial (High)

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PROFESSIONAL ELECTIVE

P23VLP20	LOW POWER VLSI DESIGN	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design

COURSE OBJECTIVES:

- To learn the types of power dissipation and low power synthesis
- To study the concepts of low power arithmetic circuits and static RAM architectures
- To understand the energy recovery techniques used in low power design

UNIT I POWER DISSIPATION IN CMOS 9

Sources of power dissipation – Physics of power dissipation in MOSFET devices – The MIS structure – Long channel MOSFET– Submicron MOSFET and gate induced drain leakage – Power dissipation in CMOS – Short circuit dissipation – Dynamic dissipation and load capacitance

UNIT II SYNTHESIS FOR LOW POWER 9

Behavioral level transforms – Algorithm level transform – Circuit activity driven architectural transformations – Operation reductions – Operation substitutions – Logic level optimization

UNIT III CIRCUIT LEVEL OPTIMIZATION 9

Introduction – Circuit level transform – Gate delay model – Switching event probabilities – Power consumption of CMOS – Characterization of gates – Transistor reordering – Transistor sizing – Future directions

UNIT IV LOW POWER SUB SYSTEM DESIGN 9

System power management support – Compatibility constraints – Supply voltage for standby – Architectural trade-off for power – Instruction set architecture – Instruction execution pipeline – Data paths-cache effects – Clock distribution – Clock gating

UNIT V LOW ENERGY COMPUTING USING ENERGY RECOVERY TECHNIQUES 9

Energy dissipation in transistor channel using an RC model – Energy recovery circuit design – Designs with partially reversible logic – Supply clock generation

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI circuit design, John Wiley and Sons Inc, 2nd edition, Reprint-2014
2. K.S. Yeo and K.Roy, "Low Voltage Low Power VLSI Subsystems", 2nd edition, Tata McGrawHill, 2016

REFERENCES:

1. Jan M.Rabaey, MassoudPedram, Low power Design methodologies,Springer US, 1st Edition, 2014
2. Soudris, Dimitrios, ChristrianPignet, Goutis, Costas, Designing CMOS circuits for low power, Springer US, 1st Edition, 2011
3. Gary K.Yeap, Practical Low Power Digital VLSI Design, Springer US, 1st Edition 2010
4. AjitPal, Low Power VLSI circuits and Systems, Springer India, 1st Edition, 2014

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Interpret the concept of low power design methods	Understand
CO2	Compare the logic level and circuit level Optimization of circuits	Understand
CO3	Apply low power techniques in circuit level.	Apply
CO4	Explain the low power sub system design	Understand
CO5	Inspect the low energy computation using appropriate energy recovery technique	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2.4	1.6	1.4	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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