

## Webinar on

# VLSI Design using Verilog HDL

The Webinar on “VLSI Design using Verilog HDL” was conducted by Founder and CEO of Maven Silicon, Mr.P.R.Sivakumar on 12<sup>th</sup> Sept. 2019. The target audience were 24 students attached with SIG-VSP. The webinar was designed and delivered with a combination of video lectures and labs to empower the students with an all round understanding of the subject. The webinar was completely relay on Verilog programming. Initially he gave an overview of VLSI design that includes how to design SoC and what is the difference between ASIC and FPGA. He also covered RTL design using Verilog programming of some basic circuits. Under the Data types in Verilog he gave a complete overview of data type concepts, Nets, registers, Non hardware equivalent variables and arrays. He also emphasized on Verilog operators, which includes logical operators, bitwise, reduction operators, concatenation ,conditional operators, relational, arithmetic, shift and equality operators. After the webinar session, students posted many quires and all the questions were addressed to the point. Students after the session practiced on Verilog programming with the help of the internal faculties to enrich the knowledge in Verilog HDL. This webinar is useful in designing the projects using Verilog HDL.

